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FPGA IMPLEMENTATION OF 8-BIT PARALLEL CYCLIC REDUNDANCY CODE

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ABSTRACT

This paper presents a different ways to solve the parallel CRC circuit. Certain drawbacks were observed in the without FPGA board. Some techniques used Linear feedback shift registers (LFSR) to do serial implementation. This origin resulted in a circuit that was inefficient in terms of time utilization because of parallel communication. We have worked on the related problems and have proposed an efficient mechanism. We have improve the VHDL code using VHDL structural modeling. The work was also compared with existing models of parallel implementation of eight bit CRC circuit. The code is written for eight bit parallel CRC and FPGA implementation of the code was done. Comparing with existing work, the model is more efficient in terms of hardware utilization. As the hardware utilization has been done in an efficient way, the overall efficiency of the parallel CRC is found to develop.

KEYWORDS: PARALLEL CRC, CRC, STRUCTURAL MODELLING.

1. INTRODUCTION

CRC (Cyclic Redundancy Check) is the subset of linear block codes. It is mainly used in data storage, communications, control system and industrial measurement. The evolving world of telecommunications requires speed in communications and increasing reliability. The Cyclic Redundancy Check (CRC) was invented by W.Wesley. CRC is an error detecting code and which is used to detect an error in the message bits. This error is received at the receiver side by sender which is transmitter. The hardware mapping problem of the parallel CRC computation was first addressed by Braun which was based on the matrix computation technique which is different from Pei. There are two types of codes which are the-: block codes and the other is convolution codes. Both of them introduce the redundancy by adding parity bits to the message bits. The main applications of CRC is detecting errors in data communication systems and devices for storage. Integrity of blocks of data called Frames is also verified.

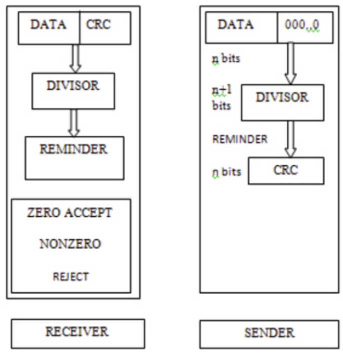
2. CALCULATION OF CRC

CRC uses binary division technique. A sequence of redundant bits are called as CRC or the CRC remainder are origin at the end of the message bits so that the resultant data which include the message bits and the redundant bits is divisible by a second predetermined number which is binary.

Firstly, a string of m 0's is appended at the end of the message bits. The bits that we are adding is m. It is less than the bits in the divisor which is m+1 by one. Secondly, the resultant bits are divided by the divisor using the binary division method. The remainder generated is the CRC. Thirdly, the CRC generated is added to the data unit by replacing the redundant bits. The data unit is checked at the receiver side. Now the data unit which include the message bit and the CRC is again divided by the same divisor known both to sender and receiver by using binary division. If the remainder is zero then message sent is without error else error is there in the message.

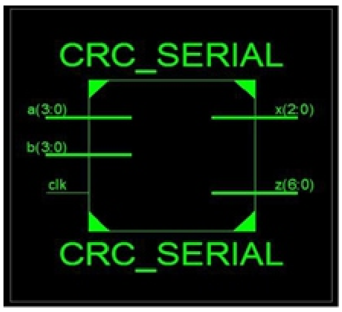
3. PARALLEL CRC COMPUTATION ALGORITHM

1. The F matrix is generated with the help of generator polynomial.
2. The message is fed as input and the bits are fed parallel.
3. These parallel bits are multiplied bitwise with the F matrix.
4. Initially the value of FCS is set as zero by clearing all the LFSRS .
5. The output obtained from STEP3 is Exhorted with the previous value of FCS.
6. Then new FCS is obtained which is fed back.
7. Now the new value of FCS is calculated by Exuding the output from STEP3 and the FCS value which is fed back.
8. The final value of FCS will be obtained after (k+m)/w cycles.

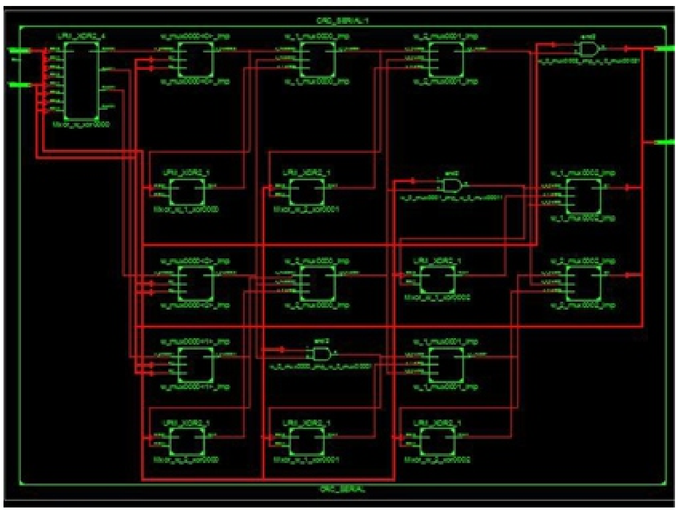


4. RTL SCHEMATIC

1. RTL Schematic of serial CRC



2.RTL Schematic of parallel CRC



5. CONCLUSION AND FUTURE SCOPE

Calculation of CRC (Cyclic Redundancy Check Code) forms an important aspect in determining the speed of any communication system. We studied the various methods for generation of CRC. We also analyzed the work done by various researchers in this field. We found out that a lot of work has been done in this field regarding speed of the circuit, choosing generator polynomial, hardware architecture etc. However, later it was realized that this was not an efficient method. So, later the work was shifted towards the parallel architecture. In our project work, we have focused on developing an efficient VHDL code for the parallel implementation of the CRC circuit. We developed VHDL code using serial as well as parallel architecture and found out the time delay in both the cases. The delay was reduced to almost half in the parallel architecture and thus we developed an efficient code for optimizing the speed of the circuit.

Out of the various research papers, we found that some researchers were able to optimize speed by minimizing hardware, while some achieved the desired performance by improving their code. Initially Serial Linear Feedback Shift Registers (LFSR) were used to design the CRC code. Later on, it was realized that using Serial LFSR had its own limitations. It could process only one bit at a time in a single clock pulse. So optimum speed was not achieved. To overcome this all limitation parallel implementation of LFSRs was done by many researchers. As a result the speed of the circuit improved greatly. It although some researchers achieved good speed as high as 35-40Gbps. It is the method was applicable only for particular CRC. On the other hand, some researchers did develop codes for CRCs of different length but the desired speed could not be achieved.

The F matrix which we have used in our code is only applicable for eight bit CRC.

However, the code for F matrix for higher bit CRCs, rather a generic code for matrix can be written. Also the hardware complexity can be further minimized using loops to minimize the code.

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